

# Very-Long Instruction Word

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## 1 Summary

This article explain about a different type of architecture os microprocessor. This is different from the traditional RISC and CISC architecture. This is a interessant article for those who like processor architecture and high performace studies. It explain how the VLIW architecture works and why it is better for superscalar processor. It shows why it transfer the complexity from the hardware to the software.

This kind of architectures was created focused on high performance. The main difference between this achitecture and CISC and RISC architectures is the easiest way to explore paralelism from aplications just using the hardware.

The main goal of VLIW is the superscalar processing. The hardware needed is simplier than on a RISC or on a CISC architecture. CISC architectures are the complex structure for building superscalar processor, because this kind has a instruction set with different size of code. It can vary from one to four. In this case all hardware must be modified to predict were, in the code, we have cases of paralelism. Although we need more complex hardware to undo some instructions that have been predicted wrongly.

RISC has a huge advantage over CISC for the creation of superscalar processors. RISC has a simpler set of instruction with fized size that makes pipelining and command prediction easier. All the hardware is much more simpler than the CISC superscalar processor.

In the VLIW architecture we do not need the complex system of prediction and reordering buffer. This happen because it let all the complexity in the hands of the compiler. With this we have a cheaper circuit and makes chips smaller.

When we have the complexity on the software we change the paradigm. The software can be rewritten to makes the prediction better. All the modification depends only of the compiler let the processor unchenaged. If we had to change the processor, the old ones would be trew away. All this makes things cheaper.

This structure is faster than the others and allow a better pipelining executing multiples instructions at the same time.

### 1.1 Comparison

This section will describe a comparison between the different architectures.

#### 1.1.1 Instruction Size

On CISC we have instruction with different sizes, from one to four bytes. On RISC we has always the same size of instruction and this makes things easy. On VLIW we have twelve bytes of instruction. The first four is for decision make and jump conditions. The second four is for ULA (arithmetic operations) instructions. And the last one is for read or write operations.

### **1.1.2 Registers**

On CISC we have few registers a some of special pourpose. In the other two we have a lot of general pourpose register.

### **1.1.3 Memory Reference**

On CISC we have a lot of operations concerning memory. This makes a complex set of instruction. The other ones we just have read and write, turning all simpler.